Multimedia Research Lab
Lahore University of Management Sciences

Project: Power Aware Video Codec-Phase 1

PI: Dr. Nadeem Ahmad Khan
Co-PI: Dr. Jahangir Ikram

Platforms and Tools

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Prepared by: Tayyab Naseer, Zahaib Akhtar
Contents

SECTION 1: Overview of Mobile Devices ................................................................. 5
1.1 Introduction ...................................................................................................... 5
2.1 Detailed List of Embedded Devices ................................................................. 5
  2.1.1 Personal Digital Assistants ...................................................................... 5
  2.1.2 Mp3 players ............................................................................................ 6
  2.1.3 Digital Cameras ...................................................................................... 6
  2.1.4 Video Game Consoles ............................................................................ 6
  2.1.5 Mobile Phones ....................................................................................... 6
  2.2 Conclusions: ............................................................................................... 6

SECTION 2: Embedded processors used in mobile devices and evaluation boards ....... 8
3.1 A brief note on the ARM Processors ............................................................... 8
3.2 Texas Instruments C55xx™ processors and TI C5510 DSK ......................... 9
3.3 Texas Instruments C64xx™ processors and TI C6411 DSK ......................... 9
4.1 OMAP Processors and their Evolution: ......................................................... 10
  4.1.1 OMAP Architectural Diagram for OMAP 1710 ...................................... 11
  4.1.2 OMAP2420 and its Portability ............................................................... 12
  4.1.3 Configurations of DSP/BIOS in OMAP 2420 ....................................... 12
    4.1.3.1 Overview ......................................................................................... 12
    4.1.3.2 OMAP 2420 and the CLK Module ................................................. 12
    4.1.3.3 GEL Configuration ....................................................................... 13
    4.1.3.4 OMAP 2420 and the HWI Module ................................................. 13
    4.1.3.5 OMAP 2420 and the C55 Module ................................................. 13
  4.2 VPOM 2420 ............................................................................................... 14
4.3 OMAP 3 Platform ......................................................................................... 16
4.4 OMAP 4xxx Platform .................................................................................. 18
5.1 OMAP 3530 Evaluation Module ................................................................. 20
5.2 OMAP 3530 BeagleBoard: A Cheap Alternative ......................................... 21
6.1 Conclusions ............................................................................................... 24
7.1 Reference ..................................................................................................... 25
Section 1 Overview of Mobile Devices

1.1 Introduction

An embedded system is a computer designed to perform a specific task often with the constraints of time, in order to produce the output in real time. Embedded systems are controlled by a main processor that is either typically a microcontroller or a DSP (Digital Signal Processor)

Below is a list of some embedded applications used commonly:

- Personal Digital Assistants
- Mp3 players
- Digital cameras
- DVD players
- Video game consoles
- Mobile Phones

The processors for these devices are manufactured by various companies such as Texas instruments, Samsung, PortalPlayer and Nvidia to name a few. Some detail about embedded devices and their processors is provided as follows:

2.1 Detailed List of Embedded Devices

2.1.1 Personal Digital Assistants

Following is a list of some PDAs

- Abacus PDA Wrist Watch with Motorola DragonBallVZ Series
- Acer N Series with Samsung S3C2410
- Apple Inc.'s iPhone & iPod Touch with PortalPlayer and Samsung Processors
- BlackBerry with ARM9 chips, (manufacturer not known)
- I-mate with Qualcomm MSM7200
- Nokia E-Series with Texas Instrument OMAP 1710
2.1.2 Mp3 players

- iPod with PortalPlayer and Samsung Processors

2.1.3 Digital Cameras

- Canon 5D series with Canon Digic 4 Processors
- Nikon D3 camera with Nikon EXPEED processors

2.1.4 Video Game Consoles

- Xbox 360 with IBM Power-PC
- Playstation 3 with Power-PC @ 3.2 GHz
- Nintendo DS with ARM 9 @ 67 MHz (make and model not disclosed)

2.1.5 Mobile Phones

- Sony Ericsson P990i with ARM-9 Processors (make and model not disclosed)
- HTC (High Tech Computer Corporation) Tornado with TI OMAP 850
- Motorola CLIQ MB200 with Qualcomm MSM7201A
- Samsung phones use various Processors manufactured by Samsung itself and TI OMAPs
- Nokia N-Series with TI OMAP 2420

2.2 Conclusions:

It can be safely concluded that Texas Instrument's OMAP processors have wide usage in terms of mobile computing as can be seen from the above applications, a number of them are using these processors such as Nokia N-series and different Samsung
manufactured mobile phones, hence it would be a very suitable processors platform for the development of the prototype for the project.
SECTION 2: Embedded processors used in mobile devices and evaluation boards

3.1 A brief note on the ARM Processors

“The ARM is a 32-bit reduced instruction set computer (RISC) instruction set architecture (ISA) developed by ARM Limited. It was known as the Advanced RISC Machine, and before that as the Acorn RISC Machine. The ARM architecture is the most widely used 32-bit ISA in terms of numbers produced. They were originally conceived as a processor for desktop personal computers by Acorn Computers, a market now dominated by the x86 family used by IBM PC compatible computers. But the relative simplicity of ARM processors made them suitable for low power applications. This has made them dominant in the mobile and embedded electronics market as relatively low cost and small microprocessors and microcontrollers.

As of 2007, about 98 percent of the more than a billion mobile phones sold each year use at least one ARM processor. As of 2009, ARM processors account for approximately 90% of all embedded 32-bit RISC processors. ARM processors are used extensively in consumer electronics, including PDAs, mobile phones, iPods and other digital media and music players, hand-held game consoles, calculators and computer peripherals such as hard drives and routers.

The ARM architecture is licensable. Companies that are currently or formerly ARM licensees include Alcatel, Atmel, Broadcom, Cirrus Logic, Digital Equipment Corporation, Freescale, Intel (through DEC), LG, Marvell Technology Group, NEC, NVIDIA, NXP (previously Philips), Oki, Qualcomm, Samsung, Sharp, ST Microelectronics, Symbios Logic, Texas Instruments, VLSI Technology, Yamaha and ZiiLABS.” (Wikipedia.com).
3.2 Texas Instruments C55xx™ processors and TI C5510 DSK

The TMS320VC5510/5510A (5510/5510A) fixed-point digital signal processors (DSPs) are based on the TMS320C55x DSP generation CPU processor core. The C55x™:DSP architecture achieves high performance and low power through increased parallelism and total focus on reduction in power dissipation. The CPU supports an internal bus structure composed of one program bus, three data read buses, two data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to three data reads and two data writes in a single cycle. In parallel, the DMA controller can perform up to two data transfers per cycle independent of the CPU activity.

The DSK features the TMS320C5510 DSP, a 200 MHz device delivering up to 400 million instructions per second (MIPs) and is designed for products that require an optimized combination of power, performance and area. The C5510 is based on the industry’s lowest power TMS320C5000 DSP platform and is ideal for applications such as digital audio players, digital still cameras, electronic books, portable medical devices, voice recognition, GPS receivers, fingerprint/pattern recognition, wireless modems, headsets, and biometric. The TMS320C5510™ DSP Starter Kit (DSK) developed by Spectrum Digital is a low-cost development platform designed to speed the development of power-efficient applications based on TI’s TMS320C55x DSP generation. TI’s new power management tools allow developers to evaluate system power and examine the frequency-voltage scaling feature for future revisions of the TMS320C5510 DSPs. Designers can evaluate the Power Analyzer and Power Scaling Library to confidently tune their systems to maximize efficient power consumption in applications ranging from portable internet appliances to high speed wireless communications.

3.3 Texas Instruments C64xx™ processors and TI C6411 DSK

The TI C64xx series is family 16 bit fixed point VLIW DSP processors from Texas instruments. Its instruction set is the superset of the TI C62xx architecture and adds
significant SIMD (Single instruction multiple-data) capabilities among other enhancements. It targets high performance applications like video, imaging, wireless base stations and radar and sonar systems. With performance of up to 5760 million instructions per second (MIPS) at a clock rate of 720 MHz, the C64x devices offer cost-effective solutions to high-performance DSP programming challenge.

TMS320C6416 DSP Starter Kit (DSK) is a low-cost development platform designed to speed the development of high performance applications based on TI’s TMS320C64x DSP generation. The C6416 DSK tools include the latest fast simulators from TI and access to the Analysis Toolkit via Update Advisor which features the Cache Analysis tool and Multi-Event Profiler. Using Cache Analysis developers improve the performance of their application by optimizing cache usage. By providing a graphical view of the on-chip cache activity over time the user can quickly determine if their code is using the on-chip cache to get peak performance. The DSK features the TMS320C6416 DSP, a 1 GHz device delivering up to 8000 million instructions per second (MIPs) and is designed for products that require the highest performing DSPs. The C6416 is based on the high performing TMS320C6400 DSP platform designed to needs of high-performing memory intensive applications.

4.1 OMAP Processors and their Evolution:

TI has periodically released updates to its OMAP processors platform series starting from OMAP Integrated Modem and Applications Processor, these were the earliest processors in this family and were adopted by various Mobile Phone manufacturing companies, the family included OMAP 850, OMAP V1030 and OMAP V1035. The next generation was that of OMAP DM-CoProcessors, these were followed by the OMAP 1 Processor generation which became widely used in mobile computing such as Nokia E-Series, the family featured the OMAP 1710 Processors, the architecture level diagram of the processor is as shown below:
The next generation in the processor family is the OMAP 2 Processor released by TI in the year 2005. The family featured the OMAP 2420 and the OMAP 2430/2431. The processor was widely adopted by many Mobile phone manufacturing companies. The figure below shows the architecture level diagram of the processors.
4.1.2 OMAP2420 and its Portability
Texas instruments have developed various DSP processors and other platforms for different and specific purposes. TI C55xx DSP processors are low power DSPs and platforms like OMAP2420 is a category of proprietary microprocessors that have capabilities for mobile multimedia applications. Many mobile phones use OMAP microprocessors including most of Nokia’s N series mobiles. Main emphasis of our project is to optimize the application for power so we need to profile the power consumption of the embedded device. For the said purpose we will be developing our application on TI C5510DSK and later on we will try to port the application onto the OMAP2420 to show the feasibility that our application meets the demand of commercially developed handheld devices which often use OMAP microprocessors. This report comments on the changes you will have to make

4.1.3 Configurations of DSP/BIOS in OMAP 2420
I will address some of the enhancements in the OMAP 2420 architecture and configurations to be done for DSP/BIOS of OMAP 2420.

4.1.3.1 Overview
DSP/BIOS has been enhanced to provide seamless support for the General Purpose Timers (GP Timers) and Level 2 Interrupt Controller (L2IC) present within the OMAP 2420. The CLK module functionality is now driven by GP Timers. The HWI module APIs can define and manipulate level 2 interrupts in addition to level 1 interrupts. The OMAP 2420 is the first in a series of next generation "OMAP 4" devices. This series may also be referred to as OMAP24xx devices.

4.1.3.2 OMAP 2420 and the CLK Module
A number of changes and enhancements have been made to the DSP/BIOS CLK module to enable the use of OMAP 2420 General Purpose (GP) timers. The OMAP 2420 has 12 General Purpose (GP) timers. Four timers (5, 6, 7, and 8) are designed to be used by the DSP.
4.1.3.3 GEL Configuration

In order for the DSP to access the GP timers, you must configure the DSP MMU to map the GP timers into the DSP address space. This can be done using the following ARM-side GEL commands (which are also provided with CCStudio) or dedicated ARM code.

4.1.3.4 OMAP 2420 and the HWI Module

With the introduction of the OMAP family of dual-core ARM + ‘C55x devices, many more interrupt sources have been defined than can be terminated on the legacy ‘C55x level 1 interrupt controller, which has a limit of 32 interrupts. To accommodate additional interrupt sources, a new interrupt mechanism has been provided in hardware: the "Level 2 Interrupt Controller" (L2IC). The additional interrupts are prioritized and multiplexed by the Level 2 Interrupt Controller onto two dedicated level 1 interrupts. DSP/BIOS internally configures all 32 level 2 interrupts to terminate on the single level 1 FIQ interrupt. In the 24xx OMAP family, many peripherals that formerly interrupted the DSP at level 1 have been moved out to level 2.

The L2IC contains a 32-bit Interrupt Mask Register (MIR), which defines which level 2 interrupts are enabled or disabled. The DSP/BIOS interface to the L2IC is implemented as part of the HWI module.

4.1.3.5 OMAP 2420 and the C55 Module

In addition to extensions to the HWI module, the following extensions have been made to the C55 module to support the OMAP 2420 level 2 interrupts.

4.1.3.5.1 C55_plug API

For C55_plug, the range of vector IDs is extended from 0-31 to 0-63. The IDs 32-63 correspond to level 2 interrupts 0-31 respectively. The c55.h file now includes definitions C55_L2_INT0 through C55_L2_INT31 which map to vector IDs 32-63.
4.1.3.5.2 New APIs

The following APIs have been added to the C55 module for use with OMAP 2420.

C55_disableInt. Disable an individual interrupt.
C55_enableInt. Enable an individual interrupt.
C55_l2AckInt. Explicitly acknowledge an L2 interrupt
C55_l2DisableMIR. Disable a mask of L2 interrupts
C55_l2EnableMIR. Enable a mask of L2 interrupts
C55_l2SetIntPriority. Set the priority of a L2 interrupt

4.2 VPOM 2420

This virtual platform is a high performance software simulator of the TI OMAP2420 Software Development Platform (SDP2420) designed for advanced mobile phone video and imaging development. OMAP2420 is based on the OMAP2 architecture that includes the ARM11 and C55xx DSP. The VPOM-2420 powers dramatic gains in developer productivity by integrating with the software developer’s preferred development environment for application, middleware, operating system and driver development, making it a feasible alternative even after silicon development boards have become available.
The OMAP 2420 processor employs an ARM 11 core with a C55x DSP along with a dedicated Graphics Accelerator, enhancements have also been made to the imaging and video accelerator for high resolution still capture applications, multi-megapixel cameras and full-motion video encode and decode with VGA resolution of 30 frames per second.

The OMAP 2420 for this all round ability has been a popular processor with the mobile phone manufacturers and following is the list of Mobile Phones using the processor.
Mobile Phone Manufacturers using OMAP 2420 and OMAP 2430/2431

<table>
<thead>
<tr>
<th>Nokia</th>
<th>Motorola</th>
<th>Samsung</th>
<th>Others</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nokia N810 Internet Tablet WiMAX edition</td>
<td>Motorola RIZR Z10</td>
<td>Samsung SGH i616</td>
<td>Softbank X02NK</td>
</tr>
<tr>
<td>Nokia E-90 Communicator</td>
<td>Motorola MOTO Q 9H</td>
<td>Samsung SGH i617</td>
<td></td>
</tr>
<tr>
<td>Nokia N93, Nokia N93i and Nokia N93i-5</td>
<td></td>
<td>Jack</td>
<td></td>
</tr>
<tr>
<td>Nokia N82</td>
<td></td>
<td>Samsung SGH i617</td>
<td></td>
</tr>
<tr>
<td>Nokia N95 8GB</td>
<td></td>
<td>BlackJack II</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Samsung GT-i7110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Samsung GT-i8510</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>INNOV8</td>
<td></td>
</tr>
</tbody>
</table>

Various Mobile phone manufacturers using OMAP 2420, OMAP 2430/2431 Processors

4.3 OMAP 3 Platform

The next generation of the processors added to the family is the OMAP 3 Processor Platform. These processors are endowed with even greater multimedia processing power with specialized core to perform image and video processing. The processors have not yet been widely adopted by many mobile manufacturers as they have been released much recently and not a lot of companies have been able to yet tap into OMAP 3 Processors power. However, the trend suggests that in the coming years these processors will be forming the backbone of many Smartphones and will be a significant addition to the embedded devices’ ever increasing power. The OMAP 3 Processors employs a state of the art ARM 8 Cortex Core with a specialized TMS320C64x core
from TI to process video and image data. A separate graphical accelerator is also built in to the hardware, so that vector processing for the purpose of screen display can be performed in a specialized manner. Similarly a specialized Image and Video Accelerator is built into the hardware. The OMAP 3 Processor family features the **OMAP 3410, OMAP 3420, OMAP 3430, OMAP 3440, OMAP 3610, OMAP 3620, OMAP 3630 and OMAP 3640** Processors.

The architectural level diagram detailing the significant features of the OMAP 3 Processor is given on the following page. The diagram is that of the OMAP 3440 processor, all the other processors in the family share the same hardware characteristics, the only difference is between the operating frequencies of the cores.

Architectural Diagram of OMAP 3 Platform
The OMAP3440 leverages TI’s high performance IVA 2+ multimedia accelerator to support 720p HD video record and playback, unleashing user creativity behind the lens. Additionally, at the heart of the OMAP3440 is a superscalar ARM® Cortex™-A8 that provides 800 MHz of performance to enhance applications that take advantage of the larger displays used in MIDs.

One of the first mobile phones using the processor is the Palm’s Pre. In TI’s release of the OMAP 3 platform processors the mobile company NEC showed interest in adapting the processor for their future mobile phones, which marks a positive sign for the processor and its possible usage. Therefore keeping this future possibility in mind it would be a good idea to use this processor for the project.

4.4 OMAP 4xxx Platform

The next processor generation is OMAP 4 Processor platform, TI has announced its release on the 16th of February 2009, however their usage in mobile computing seems far away due to the recent release of OMAP 3 Processors. Therefore no evaluation boards for the platform are available the moment from TI. The architectural diagram is the following
This processor family includes the **OMAP 4430** and the **OMAP 4440**.
5.1 OMAP 3530 Evaluation Module

The evaluation module for OMAP 3 is readily available from TI's website. Designed with a modular and extendable architecture, the OMAP35x EVM consists of three interconnected boards that form the complete system. The following is an overview of what is on each board.

OMAP35x EVM Main Board:

- 3.7" VGA/QVGA touch screen LCD display supporting landscape/portrait modes
- NEW! Camera connector to support third party CMOS Sensors
- NEW! S-Video/Component/Composite input, S-Video output
- High Speed USB 2.0
- Daughter card connections to most peripheral interfaces
- 10/100Mbps Ethernet, SDIO, I2C, JTAG, Keypad
- High-speed MMC/SD

OMAP35x EVM Processor Module:

- Speed optimized OMAP3530 processor (720MHz ARM Cortex-A8 / 520MHz C64x+ DSP)
- 256 MB LPDDR/256 MB NAND Flash

OMAP35x EVM Power Module:

- TPS65950 Integrated Power Management IC that supports the power and peripheral requirements of the OMAP35x application processors

The photograph of the evaluation board is given on the next page.
5.2 OMAP 3530 BeagleBoard: A Cheap Alternative

The OMAP 3530 BeagleBoard is a joint product of DigiSys and Texas Instruments. It has the exact same hardware specifications as that of the OMAP 3530 EVM and comes with development tools developed in Linux. The board is available at a very cheap price compared to that of the EVM. The BeagleBoard does not give the user the luxury of the LCD display that is available on the OMAP evaluation module as can be seen from the picture, there is also no support for direct interfacing of a data capture device such as a camera, however, the rest of the hardware specifications are the same as can be seen from the block level diagram of the two boards.
The board as stated above is based on the OMAP 3530 processor, the next figure gives a high level diagram of the processor and features available as on the board.
The next figure shows the features as available on the OMAP 3530 evaluation board.
The OMAP3503, OMAP3515, OMAP3525 and OMAP3530 applications processors were released in August 2008 as reported on the following website link, the OMAP 36x family was scheduled to be released in the last quarter of year 2009

http://embedded-system.net/omap3503-omap3515-omap3525-omap3530-processors-omap35x-dv sdk.html

Memory on the boards can be added via the expansion slots available on both the boards. Support for flash memory is also available.

6.1 Conclusions

Above documentation summarizes two aspects, one is which processor to use which will provide the perfect environment to develop the video codec for the embedded mobile devices. Secondly how to port codecs which are developed on evaluation boards to the commercially used platforms.

The OMAP 3530 Evaluation board if used in the project will provide with the following advantages:

- By the time of the conclusion of the project, TI OMAP 3 Processor platform will be a popular processor in terms of mobile computing.
- Built for Linux platform, therefore issues of compiling Ffmpeg and Xvid on windows will not be there.
- Evaluation board will provide an opportunity to test the prototype and report results in real time.
- Memory available on board fulfills the requirement, support to add more memory to the board is also available.

Hence the above said platform is a good candidate for usage in the project. Once insight has been developed in the codec and its modules it will be a good time to map the codec on to the evaluation board for testing of the prototype.

All of the above documentation targets the enhancements and configurations for the DSP/BIOS of OMAP 2420. These are some of the changes we will have to make while moving from TI C5510 to OMAP 2420. Technical support of TI was contacted about the
portability issue and they said above mentioned changes are the only changes we will have to make while switching to OMAP 2420. Still complete portability of the application from C5509 DSK to OMAP 2420 is questionable as no technical document regarding this query was found. Other option is that you can test or develop your application for the OMAP 2420 environment by using VPOM 2420.

7.1 Reference

Detailed configurations and examples of usage is available on the following link

http://focus.ti.com/lit/ug/spru404n/spru404n.pdf

Note: Refer to appendix D of the above document


http://focus.ti.com/docs
Section 3: Survey of power profiling tools

8.1 Introduction

As the title of our project suggests, our video codec has to be power aware and adaptive to the battery status of the portable device. In the preliminary stages of our project we have to download and test the complexity of existing open source Video Codcs. Power consumption can be taken in different contexts. Some take power consumption proportional to complexity of the algorithm, some define a mapping function between complexity and power consumption. Real time hardware based current consumption measurement is also performed to get the actual idea of power drainage of the battery to estimate its life and take measures based on its status.

8.2 Simulators

There are two main types of performance simulators for processors.

I. Trace Driven
II. Execution Driven

Trace Driven simulators use traces obtained from real execution of programs to drive a performance model while execution driven simulators simulate the actual execution of program recording detail performance statistics.

For analysis of power consumption simulators have been developed on user level and architectural level. They are tabulated in the following table.
<table>
<thead>
<tr>
<th>User Level</th>
<th>Architecture Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple Scalar</td>
<td>SimWattch</td>
</tr>
<tr>
<td>MINT</td>
<td>Wattch</td>
</tr>
<tr>
<td>Rsim</td>
<td>Simple Power</td>
</tr>
<tr>
<td>Shade</td>
<td></td>
</tr>
</tbody>
</table>

Table 1.1: List of Simulators

8.2.1 SimpleScalar
- Designed to measure the performance of several parts of superscalar processor
- Open source project, no license required for non-commercial use
- Runs on Unix platforms
- The tool set takes binaries compiled for the SimpleScalar architecture and simulates their execution on one of several provided processor simulators.
- The advantages of SimpleScalar are high flexibility, portability, extensibility and performance.
- GNU tools need to be installed on the host system
- The simulator executes user level code

All the details regarding the installation and usage about SimpleScalar toolset can be found on the following links

http://www.simplescalar.com
http://www.simplescalar.com/docs/users_guide_v2.pdf/

8.2.2 Shade
- Shade is an instruction set simulator and custom trace generator
• Application programs are executed and traced under the control of a user-supplied trace analyzer.
• Current implementations run on SPARC and MIPS I instruction sets.
• Shade combines efficient instruction-set simulation with a flexible, extensible trace generation capability. Efficiency is achieved by dynamically compiling and caching code to simulate and trace the application program.

Source


8.2.3 SimplePower

• SimplePower is an execution driven, cycle-accurate RT level energy estimation tool that uses transitive sensitive energy models for in-order 5-stage pipelined datapath
• Perfect cache is assumed for this release
• SimplePower is tested only on Unix running Sun machines

Limitations

• Perfect cache is assumed for this release
• Integer divisions are not implemented
• Clock power is not implemented
• Floating point instructions are not implemented
• System calls are not implemented

Details about installation of SimplePower and simulating your benchmarks are explicitly described in the following hyperlink

http://www.cse.psu.edu/~mdl/software.htm
8.2.4 WATTCH

Wattch is a framework for architectural-level power analysis and optimizations. It is used as the power analyzer at the architectural level. It provides the researchers power efficient computing environment by providing a power evaluation methodology within the portable and familiar SimpleScalar framework.
Power models are interfaced with SimpleScalar, which keeps track of which units are accessed per cycle and records the total energy consumed for an application.
References

http://www-unix.ecs.umass.edu/~bdatta/SP06FPGA_FINAL/WATTCH.htm
http://www.eecs.harvard.edu/~dbrooks/wattch-form.html

8.2.5 SIMWATTCH

SimWattch combines two widely used simulators. SimWattch integrates Simics, a system level tool, with Wattch, a user level tool, to facilitate analysis for system developers.
All programs running on Solaris 8 can run on SimWattch. The tool plays an important role in the evaluation of power efficient architectures as well as in the development of applications.
Simwattch is an instruction-set simulator enhanced with an instruction-level power model. It estimates the actual power consumption using the proposed algorithms. Simwattch estimates the actual power consumption in a complete system simulation environment.

SimWattch simulator consists of three main components
i. Simics, a complete system level simulator. It simulates various microprocessor and peripheral devices at a functional level. Simics dynamically generate instruction traces data high speed and pass them to micro architectural simulator that models performance and power at the cycle level.

ii. Wattch is an extension of SimpleScalar that evaluates power at the architectural level. The SimpleScalar toolset models a range of detailed, dynamically scheduled processors with multiple-level memory hierarchies.

iii. SCI (SimWattch control interface) implements the interface between Simics and Wattch. It is responsible for three tasks
   a. Buffering instructions executed and committed in Simics.
   b. Servicing memory accesses issued by the micro architectural simulation module
   c. Dynamically translating Dparc-v8 instructions into SimpleScalar’s native instruction set.

   • SimWaatrch runs in Linux environment.

Wattch focuses on the processor at the instruction level or functional units, caches and memory. Simics performing on the next level of abstraction incorporates more components of a complete computer system (e.g. I/O devices) into the simulator and enables monitoring of the execution of the application-level code as well as the operating system code. The functional simulator delivers speed, handing off an instruction trace for cycle-level processor modeling to WATTCH.

Important SimWattch application is measuring power and energy dissipation. It models the dynamic power consumption $P_d$ of CMOS microprocessor as

$$P_d = CV_{dd}^2 \alpha F$$

$C$ is capacitance, $V_{dd}$ is supply voltage and $F$ is the clock frequency.

Source

http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=04343378
8.3 National Instruments (NI) LabVIEW

LabVIEW (short for Laboratory Virtual Instrumentation Engineering Workbench) is a platform and development environment for a visual programming language from National Instruments. The graphical language is named "G". Originally released for the Apple Macintosh in 1986, LabVIEW is commonly used for data acquisition, instrument control, and industrial automation on a variety of platforms including Microsoft Windows, various flavors of UNIX, Linux, and Mac OS X.

Texas Instruments (TI) has made use of LabVIEW in their products in order to give the developers the power to manage the power consumption of applications that are to be developed for the C55x DSPs. One such product is the TMS320C55x DSK which comes fitted with the power measurement module on the board which is managed by labVIEW. The following features are made available to the programmers.

**Power Planning Tools:** net power consumption can be planned with device-specific power planning tools.

**Power Scaling Library:** allows voltage and frequency scaling using the power scaling library.

**Power Management in DSP/BIOS Kernel:** manage power states with DSP/BIOS power management Kernel.

**National Instruments Power Analyzer:** the DSK has built in USB power measurement hardware for power monitoring and trigger functionality for profiling power consumption during specific segments of code.
The kit provides some very key features required for the purpose of power optimization and looking inside the hardware to really understand the working. The fully integrated set of power estimation and power measurement tools enable you to accurately plan, analyze, manage and optimize real-time power consumption. The product is available for a total of US $ 485.0.

### 8.3.1 Using the TMS320C55x DSK with LabVIEW

The TMS320C55x, as discussed above, comes fitted with a USB controller for the power measurement hardware, which is directly communicating with the program execution on the board. The hardware is controlled by NI’s LabVIEW running on the computer with which the DSK is interfaced. The different tools provided by LabVIEW allow a lot of flexibility to the developers in terms of management of power and the advantages are as follows

1. By turning off the modules on the board which are not involved in running the application to be monitored we can get a very accurate estimate of the power consumption.
2. Minimum human control inputs, as the entire work is done by the components present on the board the reading obtained will be precise and accurate.
3. The fully integrated set allows easy and accurate planning of power optimizing strategies.
4. No lengthy power profiling of all the assembly instructions required as is the case in the model proposed by Russell et al.

Therefore, keeping the above advantages in mind the TMS320C55x DSK is the most efficient and accurate way of measuring the power consumption of the codec to be developed. The board is available at a cost of US $ 485.0 (excluding shipping charges) from Texas Instruments.

### 8.3.2 Online Ordering/Purchasing and Hardware Detail

The board can be purchased online from Texas Instruments website from the following link:

http://focus.ti.com/docs/toolsw/folders/print/tmdsdsk5508.html

The exact make and model number of the kit is the following
8.3.3 Technique Proposed by Russell et al.

Among the schemes that can be followed for the purpose of power estimation and measurement, it was decided in the initial meeting that the model proposed by Russell et al. is to be followed in terms of the measurement of the power dissipation and consumption. After the exploration of the TMS320VC5510DSK and working with Code Composer Studio we have come to the conclusion that the model proposed by Russell et al. can be replicated for the purpose of power measurement with some additional equipment. However, with the following disadvantages:

- The TMS320 series processors run a total of 153 assembly instructions, hence profiling the power consumption for all of them would not only be a tedious task, but also a high probability of faulty measurements will be there.

- For the purpose of power measurement, sensitive and high precision equipments such as the Oscilloscope will be required, which is costly (≈ US $ 3,000)

- The technique involves a lot of human control inputs thereby raising the amount of error induced in the procedure.

Keeping the above points in mind, this technique therefore does not qualify as a very accurate and suitable one for the project.

8.4 Conclusion

Considering all the above mentioned simulators SimWattch seems a reasonable choice of simulating our applications for power analysis. Nowadays it is widely used for the purpose as it supports the analysis of power efficient micro architecture, application and compiler design decisions. Developing our power aware codec and simulating our results using SimWattch will also provide the opportunity to compare our results in an efficient manner with the existing power aware codecs as they have used the same platform.